IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	PAPPU, Krishna K. et al.
Serial No.:	10/695,853
Confirmation No. :	6739
Filed:	October 28, 2003
For:	METHOD OF GROUPING SCAN FLOPS BASED ON CLOCK DOMAINS FOR SCAN TESTING
Art Unit:	2825
Examiner:	Parihar, Suchin
Docket No.:	03-0128 81615

CERTIFICATE OF TRANSMISSION / MAILING

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04/04/2008 / Eric James Whitesell /
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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Please enter the following appeal brief in response to the office action dated 07/24/2007 and the final rejection of Claims 1-20 in the office action mailed on 12/31/2007.

(i) Real party in interest

The real party in interest in the subject application is LSI Corporation.

(ii) Related appeals and interferences

No other prior or pending appeals, interferences or judicial proceedings are known to appellant, the appellant's legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(iii) Status of claims

Claims 1-20 stand rejected.
Claims 1-20 are being appealed.

(iv) Status of amendments

No amendments were submitted subsequent to the final rejection.

(v) Summary of claimed subject matter

In the process of generating a full-scan design of an integrated circuit, a tool is used to search through the scan chains and to group flip-flops (FIG. 1: 112, 114, 116, 118) that are driven by the same clock (FIG.1: 126), that is, flip-flops that share a common clock domain. Because flip-flops are reordered within their respective clock domains, the information produced by the search is important for disconnecting and subsequently reordering the flip-flops in a scan chain. If flip-flops from different clock domains are stitched together, then timing violations are

likely to result causing test failures and functional failures. After disconnecting the scan chains, the placement tool can place scan flip-flops anywhere on the integrated circuit die, because the scan chain is not on the critical timing path. After the placement is done, the scan chain is restitched based on the placement information of each of the flip-flops within their respective clock domains.

A typical tool previously used to search through the scan chains traces the data input port of the first scan flip-flop (FIG. 1: 112 SI) in a scan chain to the output port of the last scan flip-flop (FIG. 1: 112 Q) in the scan chain. After all the flip-flops in a scan chain have been identified, the tool traces the clock input of each flip-flop to the clock driver (FIG. 1: 102). The clock driver may be, for example, an I/O port at the top level of the integrated circuit design. A scan chain typically has 5,000 to 10,000 scan flip-flops in an integrated circuit design, which results in an equal number of traces to find the clock driver. Also, a typical design includes between 16 and 32 scan chains. As a result, a costly period of testing time is required to complete a trace and grouping of all the scan chains in an integrated circuit design (P06 L01 - P07 L04). The present invention exploits the fact that most of the flip-flops in a scan chain share a common clock domain (P08 L23-25).

Explanation of the subject matter defined in the independent claims

Independent Claims 1 and 10 recite the following steps:

(a) receiving as input a representation of an integrated circuit design (P09 L25-28; FIG. 3: 304);

(b) initializing a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells created as an empty list (P10 L01-07; FIG. 3: 306);

(c) selecting a cell in one of the common signal domains that is not included in a corresponding list of cells for any of the common signal domains (P10 L08-15; FIG. 3: 308);

(d) tracing a net from an input port of the selected cell to a signal driver (P10 L16-24; FIG. 3: 310);

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (P10 L16-24; FIG. 3: 312);

(f) tracing the net to an input port of each cell connected to the signal driver (P10 L25 - P11 L14; FIG. 3: 312); and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver (P10 L25 - P11 L14; FIG. 3: 314).

Independent Claims 19 and 20 recite the following steps:

receiving as input a representation of an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains (P09 L25 - P10 L03; FIG. 3: 304);

initializing a corresponding list of cells for each of the common clock signal domains by creating each corresponding list of cells as an empty list (P10 L01-07; FIG. 3: 306);

selecting a cell having a clock signal input that is not included in a corresponding list of cells for any of the common clock signal domains (P10 L08-15; FIG. 3: 308);

tracing a net from the clock signal input of the selected cell to the corresponding clock signal driver (P10 L16-24; FIG. 3: 310);

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver (P10 L16-24; FIG. 3: 312);

tracing the net from the clock signal input of the selected cell to a clock signal input of each cell connected to the clock signal input of the selected cell (P10 L25 - P11 L14; FIG. 3: 312); and

inserting each cell traced from the selected cell in the corresponding list of cells for the common clock signal domain clocked by the corresponding clock signal driver (P10 L25 - P11 L14; FIG. 3: 314).

In summary, a representation of an integrated circuit design, such as a netlist, is

received as input. In this example, the netlist includes a scan chain used to test the integrated circuit design. A corresponding list of cells for each common signal domain in the integrated circuit design is initialized, that is, created as an empty list.

In one embodiment, the cells are flip-flops, and a corresponding list of flip-flops is created for each scan clock domain in the integrated circuit design. A cell belonging to one of the common signal domains that is not included in a corresponding list of cells is selected. For example, each list of flip-flops may be compared with a selected flip-flop to determine whether the selected flip-flop is included in any of the lists. If so, then the comparison may be repeated for the next flip-flop, and so on, until a selected flip-flop is not found in any of the lists. A clock net is traced from a clock port of the flip-flop to a clock driver, and the flip-flop is inserted in the list of flip-flops for the scan clock domain associated with the clock driver.

In the example of FIG. 1, the clock port CP1 of the flip-flop 112 is traced to the clock driver 102, and the name of the flip-flop 112 is inserted in the list of flip-flops for the scan clock domain associated with the clock driver 102. The clock net is then traced to a clock port of each flip-flop connected to the clock driver, and each flip-flop traced from the clock net is inserted in the list of flip-flops for the scan clock domain associated with the clock driver, advantageously reducing the search time for finding other flip-flops in the same clock domain.

In the example of the clock net 126, the clock net is traced to the clock ports CP1, CP2 and CP3 of the flip-flops 112, 114 and 116 respectively and through the clock buffer 106 to the clock port CP4 of the flip-flop 118. For the clock domain CLK2, the clock net 128 is traced to the clock ports CP5 and CP6 of the flip-flops 120 and 122. The name of each flip-flop traced from the clock net is stored in the list of flip-flops for the corresponding scan clock domain. In the example of FIG. 1, the netlist names of flip-flops 112, 114, 116 and 118 are stored in the list of flip-flops for the clock domain CLK1, and the netlist names of flip-flops 120 and 122 are stored in the list of flip-flops for the clock domain CLK2 (P09 L25 - P11 L14).

(vi) Grounds of rejection to be reviewed on appeal

The following grounds of rejection citing *Beausang* (U.S. Patent 5,828,579) and *Nadeau* (U.S. Patent 6,457,161) are to be reviewed on appeal:

(1) whether the rejection of Claims 1, 10, 19, and 20 under 35 U.S.C. § 103(a) provides a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*; and

(2) whether the rejection of Claims 1, 10, 19, and 20 under 35 U.S.C. § 103(a) shows that the proposed modification of *Beausang* by *Nadeau* would result in the claimed invention.

(vii) Argument

(1) The rejection of Claims 1, 10, 19, and 20 under 35 U.S.C. § 103(a) fails to provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*

In the office action (07/24/2007), the rejection (P03 §5) alleges that *Beausang* teaches "inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15)". The rejection (P04 §5) concludes that one with ordinary skill in the art would have been motivated to make the proposed modification of *Beausang* by *Nadeau*, ". . . because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of scan cells for partitioning of scan cells into subgroups that correspond to a common signal domain in *Beausang*". The rejection (P08, §17) further alleges that providing the necessary identification of scan cells for partitioning of scan cells into subgroups that correspond to a common signal domain is lacking in *Beausang* as follows: "Beausang, in FIG, 2A at 315, then implies the ability to determine which scan chains [i.e., groups of cells or segments] are compatible with a particular clock domain [i.e. have the same clock source as another cell or cells]. However, Beausang does not explicitly

teach a method or process that can determine whether a cell has a clock domain that is identical or compatible with another cell or group of cells. This lacking step is taught by Nadeau-Dostie." Accordingly, the rejection admits that partitioning of scan cells into subgroups that correspond to a common signal domain, i.e., the same clock source, is necessary to *Beausang* and is also explicitly missing in *Beausang*.

Because the rejection alleges that partitioning of scan cells into subgroups that correspond to a common signal domain is necessary to *Beausang* but is explicitly missing in *Beausang*, it is reasonable to interpret the rejection as alleging that *Beausang* does not sufficiently disclose the necessary step of determining which scan chains have the same clock source. If the allegations made by the rejection were true, then *Beausang* would fail to satisfy the requirement of enablement under 35 USC § 112.

However, the USPTO has determined that *Beausang* met the requirement of enablement under 35 USC § 112 when the *Beausang* patent was granted. Because the USPTO has determined that *Beausang* meets the requirement of enablement under 35 USC § 112, the presumption is established that each and every step necessary to *Beausang* is disclosed sufficiently to enable one of ordinary skill in the art to make and use the invention disclosed and claimed in *Beausang*. Because each and every step necessary to *Beausang* is presumed to be sufficiently disclosed under 35 USC § 112, the allegation that *Beausang* lacks sufficient disclosure for determining which scan chains have the same clock source is shown to be false. Because the allegation that *Beausang* lacks sufficient disclosure for determining which scan chains have the same clock source is shown to be false, the argument presented by the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*. Because the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*, the rejection of Claims 1, 10, 19, and 20 fails to support a *prima facie* conclusion of obviousness that would substantiate a rejection under 35 U.S.C. § 103. *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993) (obviousness cannot be established by combining references "without also providing evidence of the motivating force which would impel one skilled in the

art to do what the patent applicant has done").

In the office action (01/15/2007), the rejection (P08 §16-17) proposes to avoid the predicament posed by Applicant's argument by insisting that the rejection was misinterpreted and that the rejection meant to point out that the lacking step is needed in the claimed invention, not in *Beausang*. If the lacking step is not needed in *Beausang* to achieve its intended purpose as alleged by the rejection, then the motivating force for making the proposed modification of *Beausang* by *Nadeau* is based on Applicant's disclosure, not on *Beausang*. Because the motivating force for making the proposed modification of *Beausang* by *Nadeau* is based on Applicant's disclosure, the rejection of Claims 1, 10, 19, and 20 fails to bear the burden of factually supporting a *prima facie* conclusion of obviousness that would substantiate a rejection under 35 U.S.C. § 103. *In re Vaeck*, 947 F.2d 488, Rev. 5, Aug. 2006 2100-126 20 USPQ2d 1438, (Fed. Cir.1991) (the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure).

Further, if the lacking step is not needed in *Beausang* to achieve *Beausang*'s intended purpose as alleged by the rejection, then the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification. Because the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*, the rejection of Claims 1, 10, 19, and 20 lacks sufficient support to substantiate a rejection under 35 U.S.C. § 103. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Kahn*, 441 F.3d 977, 986, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006) (discussing rationale underlying the motivation-suggestion-teaching requirement as a guard against using hindsight in an obviousness analysis).

(2) The rejection of Claims 1, 10, 19, and 20 under 35 U.S.C. § 103(a) fails to show that the proposed modification of *Beausang* by *Nadeau* would result in the claimed invention

Even if the rejection did provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*, the proposed modification would fail to result in the claimed invention, because only the first six of the eight steps in Claims 1, 10, 19, and 20 are alleged by the rejection to be included in the proposed modification of *Beausang* by *Nadeau*. The rejection fails to show that *Beausang* discloses the last two steps recited in Claims 1, 10, 19, and 20 of tracing the net to an input port of each cell connected to the signal driver and inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

Further, even if the rejection had included these two steps in the proposed modification of *Beausang* by *Nadeau*, the rejection fails to show that *Beausang* would benefit from such a modification to achieve its intended purpose. Because the rejection fails to show that the proposed modification of *Beausang* by *Nadeau* includes the steps recited in Claims 1, 10, 19, and 20 of tracing the net to an input port of each cell connected to the signal driver and inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver, and because the rejection fails to show that *Beausang* would benefit from such a modification to achieve its intended purpose, the rejection not only fails to provide a reasonable suggestion for the desirability of making the proposed modification of *Beausang* by *Nadeau*, but also the modification proposed by the rejection fails to result in the claimed invention. Because the modification proposed by the rejection fails to result in the claimed invention, the rejection of Claims 1, 10, 19, and 20 lacks sufficient support to substantiate a rejection under 35 U.S.C. § 103. (all claim limitations must be taught by the prior art, *In re Royka*, 490 F.2d 981, 180 USPQ 580, CCPA 1974).

The rejection of Claims 2-9 and 11-18 lacks sufficient support to substantiate a rejection under 35 U.S.C. § 103 due to their dependence from the arguably allowable independent claims.

The fee for filing an appeal brief is submitted herewith.

Respectfully submitted,

/ Eric James Whitesell /

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(viii) Claims appendix

Claim 1: A method of grouping cells for scan testing comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell in one of the common signal domains that is not included in a corresponding list of cells for any of the common signal domains;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 2: The method of Claim 1 further comprising a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 3: The method of Claim 2 further comprising a step of generating as output the corresponding list of cells for each of the plurality of common signal domains in the integrated circuit design.

Claim 4: The method of Claim 1 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 5: The method of Claim 1 comprising performing steps (b), (c), (d), (e), (f), and (g) for

cells comprising flip-flops in a scan chain.

Claim 6: The method of Claim 5 comprising performing steps (b), (c), (d), (e), (f), and (g) for one of the common signal domains that is a scan clock domain.

Claim 7: The method of Claim 6 comprising performing steps (d), (e), (f), and (g) for a net that is a clock net.

Claim 8: The method of Claim 7 comprising performing steps (d), (e), (f), and (g) for an input port that is a clock port.

Claim 9: The method of Claim 8 comprising performing steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

Claim 10: A computer readable storage medium tangibly embodying instructions for a computer that when executed by the computer implement a method for grouping cells for scan testing, the method comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell in one of the common signal domains that is not included in a corresponding list of cells for any of the common signal domains;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 11: The computer readable storage medium of Claim 10 further causing the computer to perform a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 12: The computer readable storage medium of Claim 11 further causing the computer to perform a step of generating as output the corresponding list of cells for each of the plurality of common signal domains in the integrated circuit design.

Claim 13: The computer readable storage medium of Claim 10 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

Claim 14: The computer readable storage medium of Claim 10 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for cells comprising flip-flops in a scan chain.

Claim 15: The computer readable storage medium of Claim 14 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for one of the common signal domains that is a scan clock domain.

Claim 16: The computer readable storage medium of Claim 15 further causing the computer to perform steps (d), (e), (f), and (g) for a net that is a clock net.

Claim 17: The computer readable storage medium of Claim 16 further causing the computer to perform steps (d), (e), (f), and (g) for an input port that is a clock port.

Claim 18: The computer readable storage medium of Claim 17 further causing the computer to

perform steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

Claim 19: A method of grouping cells for scan testing comprising steps of:

receiving as input a representation of an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains;

initializing a corresponding list of cells for each of the common clock signal domains by creating each corresponding list of cells as an empty list;

selecting a cell having a clock signal input that is not included in a corresponding list of cells for any of the common clock signal domains;

tracing a net from the clock signal input of the selected cell to the corresponding clock signal driver;

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver;

tracing the net from the clock signal input of the selected cell to a clock signal input of each cell connected to the clock signal input of the selected cell; and

inserting each cell traced from the selected cell in the corresponding list of cells for the common clock signal domain clocked by the corresponding clock signal driver.

Claim 20: A computer readable storage medium tangibly embodying instructions for a computer that when executed by the computer implement a method for grouping cells for scan testing, the method comprising steps of:

receiving as input a representation of an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains;

initializing a corresponding list of cells for each of the common clock signal domains by creating each corresponding list of cells as an empty list;

selecting a cell having a clock signal input that is not included in a corresponding list of

cells for any of the common clock signal domains;

tracing a net from the clock signal input of the selected cell to the corresponding clock signal driver;

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver;

tracing the net from the clock signal input of the selected cell to a clock signal input of each cell connected to the clock signal input of the selected cell; and

inserting each cell traced from the selected cell in the corresponding list of cells for the common clock signal domain clocked by the corresponding clock signal driver.

(ix) Evidence appendix

NONE

(x) Related proceedings appendix

NONE